REMARKS

Claims 59, 66, 92, and 94 have been amended. Claim 95 has been canceled. Claims 59-60, 62, 64, 66-84, and 92-94 are pending. No new matter has been introduced.

Claim 66 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite "for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." (Office Action at 2). Applicant notes that claim 66 has been amended to correct any perceived indefiniteness. Applicant submits all pending claims are in full compliance with 35 U.S.C. § 112.

Claims 59-60, 68-84, and 92-94 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Irinoda, U.S. Patent No. 5,726,499. The rejection is respectfully traversed.

The claimed invention relates to an integrated circuit structure with specific structural features obtained by a particular process methodology. As such, amended independent claim 59 recites an "integrated circuit substrate" comprising *inter alia* "a substrate," "an oxide layer formed over said substrate," and "a plurality of cylindrical contact holes formed in said oxide layer, said plurality of contact holes extending to a topmost surface of said oxide layer and having reduced sidewall striations, thereby reducing critical dimension loss between said contact holes." As recited in amended independent claim 59, "said reduced sidewall striations resulting from the application of a first power level plasma of an etching gas to said integrated circuit substrate for a first predetermined

time followed by the application of a second power level plasma of said etching gas to said integrated circuit substrate for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma."

Amended independent claim 92 similarly recites an integrated circuit substrate comprising *inter alia* a substrate, an oxide layer formed over the substrate, and "a plurality of recesses formed in said oxide layer, sidewalls of said recesses forming sidewalls of cylindrical contact holes extending to a topmost surface of said oxide layer and having reduced striations." Claim 92 recites that the plurality of cylindrical contact holes formed in said oxide layer having reduced sidewall striations result "from the application of a first power level plasma of an etching gas to said integrated circuit substrate for a first predetermined time followed by the application of a second power level plasma of said etching gas to said integrated circuit substrate for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma." Claim 92 further recites that the "substrate has a decreased critical dimension (CD) loss compared to the critical dimension loss of a substrate formed without the application of the second, higher power level plasma."

Irinoda relates to a contact structure having a ring-shaped wall member formed in a depression of an insulation layer. (Abstract). Specifically, in FIGS. 5A-5E, Irinoda discloses a method of forming a contact hole 102A having a polysilicon ring 105A positioned above the contact hole 102A, such that the diameter of the contact hole is substantially identical to the inner diameter of the ring 105A. (Col. 11, lines 34-35). The method disclosed by Irinoda includes etching a substrate having "an insulation layer 102"

and a "silicon nitride layer 104" to form a depression 103. (Col. 10, line 37 to col. 11, line 1). A polysilicon layer 105 is deposited on the surface of the silicon nitride layer 104 and within the depression 103. (Col. 11, lines 5-6). An anisotropic etching process is applied to the polysilicon layer. (Col. 11, lines 10-11). The etching stops when the surface of the silicon nitride layer 104 and the bottom of the depression 103 are both exposed. (Col. 11, lines 17-19). The etching step results in the formation of a polysilicon ring 105A, which acts as an etching mask for creating a contact hole 102A. (Col. 11, lines 32-34).

Irinoda does not disclose the limitations of claims 59-60, 68-84, and 92-95. Specifically, Irinoda fails to teach or suggest an integrated circuit substrate having "contact holes extending to a topmost surface of [an] oxide layer and having reduced sidewall striations," as recited in amended independent claims 59 and 92. Referring to FIG. 7 of Irinoda, the contact hole 102A is defined by the oxide layer 102 that contacts an aluminum electrode 201. (Col. 12, line 67). Therefore, Irinoda cannot have a contact hole "extending to a topmost surface of [an] oxide layer." For at least these reasons, Irinoda fails to disclose all limitations of claims 59-60, 68-84, and 92-94, and withdrawal of the rejection is respectfully requested.

Claims 62, 64, and 67 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Irinoda in view of Summerfelt et al., U.S. Patent No. 5,612,574 ("Summerfelt"). The rejection is respectfully traversed.

Claims 62, 64, and 67 relate to the integrated circuit substrate of amended independent claim 59, and recite that the substrate is either germanium, gallium arsenide, or a DRAM substrate, respectively.

Summerfelt relates to a semiconductor structure "using high-dielectric-constant materials and an adhesion layer." (Abstract; Title). Summerfelt teaches that "an interlevel isolation layer" and a "barrier layer" are formed over the active region and "disposed outwardly from the conductive plug." (Col. 2, lines 42-46). "[A]n oxygen-stable inner electrode is formed outwardly from portions of the interlevel isolation layer and the barrier layer." (Col. 2, lines 46-48). Summerfelt also teaches that "[A]n adhesion layer is disposed between the oxygen-stable inner electrode and the interlevel isolation layer and the barrier layer." (Col. 2, lines 48-51). In this manner, "the problems of adhesion between the oxygen-stable layer and the interlayer isolation layer in devices including such materials" are eliminated. (Col. 2, lines 29-32).

Both Irinoda and Summerfelt, alone or in combination, fail to teach or suggest an integrated circuit substrate having "contact holes extending to a topmost surface of [an] oxide layer and having reduced sidewall striations." As discussed above with respect to claims 59-60, 68-84, and 92-94, Irinoda fails to teach each and every limitation of independent claims 59 and 92. For at least these reasons, Applicant submits that claims 62, 64, and 67 are allowable.

Claim 66 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Irinoda in view of Foote el al., U.S. Patent No. 5,710,067 ("Foote"). The rejection is respectfully traversed.

Foote relates to a silicon oxime film formed by plasma enhanced chemical vapor deposition. (Abstract). The silicon oxime film is useful as an anti-refection layer during photolithography, as an etch stop, and as a protection layer. (Abstract).

Both Irinoda and Foote, alone or in combination, fail to teach or suggest an integrated circuit substrate having "contact holes extending to a topmost surface of [an] oxide layer and having reduced sidewall striations." As discussed above with respect to claims 59-60, 68-84, and 92-94, Irinoda fails to teach each and every limitation of independent claims 59 and 92. For at least these reasons, Applicant submits that claim 66 is allowable.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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